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10/714,302	11/14/2003	Andrew H. Barr	200308580-1	2112

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EXAMINER	
MCCARTHY, CHRISTOPHER S	
ART UNIT	**PAPER NUMBER**
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,302	BARR ET AL.	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 15-20* is/are rejected.

7)☒ Claim(s) *11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *response to arguments*.

DETAILED ACTION

Claims 1-5, 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Jenkins et al. U.S. Patent 6,002,868, as cited in prior office action, which was mailed on 4/20/07.

Claims 6-7, 9-10, 15-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Jenkins in view of Shaffer et al. U.S. Patent 5,619,513, as cited in prior office action, which was mailed on 4/20/07.

Claims 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, as cited in prior office action, which was mailed on 4/20/07.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Jenkins et al. U.S. Patent 6,002,868.

As per claim 1, Jenkins teaches a computer system comprising a processor; a first bus coupled to the processor; a memory; and a core electronics complex including: a memory controller coupled to the first bus and the memory (column 3, lines 24-46; column 4, lines 3-14); a first input/output (I/O) controller coupled to the first bus and configured to couple to a first set of one or more I/O devices using a first connection (column 4, lines 3-14, figure 1, wherein the line from items 130 to 128 are deemed a first connection); and a test module (column 4, lines 32-34) coupled to the first I/O controller using a second connection that is separate from the first connection (figure 1, wherein, the test module is coupled to the I/O controller by means of bridge and bus); wherein the test module is configured to provide test transactions to the first I/O controller tocause tests to be performed on the memory using the first bus (column 4, lines 32-34; column 7, line 46 – column 8, line25, wherein, multiple memories are tested).

As per claim 2, Jenkins teaches the computer system of claim 1 further comprising: an operating system; wherein the processor is configured to cause the operating system to be booted, and wherein the test module is configured to cause the tests to be performed on the memory using the first bus subsequent to the operating system being booted (column 4, lines 24-34).

As per claim 3, Jenkins teaches the computer system of claim 1 further comprising: an operating system; wherein the processor is configured to cause the operating system to be executed, and wherein the test module is configured to cause the tests to be performed on the memory using the first bus during execution of the operating system (column 4, lines 24-34).

As per claim 4, Jenkins teaches the computer system of claim 1 wherein the first bus comprises a system bus (column 3, lines 53-67).

As per claim 5, Jenkins teaches the computer system of claim 1 further comprising: a second bus (column 3, lines 53-67, figure 1, item 128) a second set of one or more I/o devices coupled to the second bus (column 4, lines 3-6, figure 1, items 142,144); wherein the core electronics complex includes a second I/O controller coupled to the first bus and the second bus (column 4, lines 3-6, figure 1, item 136).

As per claim 8, Jenkins teaches the computer system of claim 1 further comprising: a bus bridge coupled to the first bus and the first I/O controller (column 3, lines 53-67; figure 1, item 122).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6-7, 9-10, 15-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Jenkins in view of Shaffer et al. U.S. Patent 5,619,513.

As per claim 6, Jenkins teaches the computer system of claim 1. However, Jenkins does not explicitly teach providing read and write transactions for testing. Shaffer does teach providing read and write transactions for testing (column 1, lines 44-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins. One of ordinary skill

in the art would have been motivated to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins because Shaffer teaches the testing of memory modules in a system and reporting the errors therein (column 3, lines 19-31); an explicit desire of Jenkins (column 7, line 46 – column 8, line 39).

As per claim 7, Jenkins in view of Shaffer teaches the computer system of claim 6. Shaffer teaches wherein the read and write transactions comprise direct memory access (DMA) transactions (column 2, lines 50-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins. One of ordinary skill in the art would have been motivated to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins because Shaffer teaches the testing of memory modules in a system and reporting the errors therein (column 3, lines 19-31); an explicit desire of Jenkins (column 7, line 46 – column 8, line 39).

As per claim 9, Jenkins teaches a method performed by a computer system that includes a memory comprising: selecting a portion of the memory for testing during operation of the computer system; generating a test transaction in a test module coupled to an input/output (I/O) controller using a first connection that is separate from a second connection that is configured to couple the I/O controller to one or more I/O devices; the test module and the I/O controller included in a chipset coupled to the memory; and providing the test transaction to the portion through the I/O controller (see rejection 1 inclusive of the following: column 4, lines 3-14, figure 1, wherein the line from items 130 to 128 are deemed a first connection ;column 3, lines 24-46; column 4, lines 32-34; column 7, line 46 – column 8, line25, wherein, multiple memories

are tested). Jenkins does not explicitly teach using direct memory access (DMA). Shaffer does teach using direct memory access (DMA) (column 2, lines 50-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins. One of ordinary skill in the art would have been motivated to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins because Shaffer teaches the testing of memory modules in a system and reporting the errors therein (column 3, lines 19-31); an explicit desire of Jenkins (column 7, line 46 – column 8, line 39).

As per claim 10, Jenkins teaches the method of claim 9 further comprising: detecting an error that occurs in response to the test transaction; and performing a remedial action in response to detecting the error (column 8, lines 26-39).

As per claim 15, Jenkins teaches a computer system comprising: a processor; a bus coupled to the processor; a memory; a core electronics complex including: a system controller coupled to the bus and the memory; an input/output (I/O) controller coupled to the system controller and configured to couple to a set of one or more I/O devices using a first connection; and a test module coupled to the I/O controller using a second connection that is separate from the first connection; wherein the test module is configured to provide test transactions to the I/O controller to cause tests to be performed on the memory (see rejection 1 inclusive of the following: column 4, lines 3-14, figure 1, wherein the line from items 130 to 128 are deemed a first connection ;column 3, lines 24-46; column 4, lines 32-34; column 7, line 46 – column 8, line25, wherein, multiple memories are tested). Jenkins does not explicitly teach using direct memory access (DMA). Shaffer does teach using direct memory access (DMA) (column 2,

lines 50-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins. One of ordinary skill in the art would have been motivated to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins because Shaffer teaches the testing of memory modules in a system and reporting the errors therein (column 3, lines 19-31); an explicit desire of Jenkins (column 7, line 46 – column 8, line 39).

As per claim 16, Jenkins in view of Shaffer teaches the computer system of claim 15. Jenkins teaches it further comprising: an operating system; wherein the processor is configured to cause the operating system to be booted, and wherein the test module is configured to cause the tests to be performed on the memory subsequent to the operating system being booted (column 3, lines 24-39; column 4, 32-34). Jenkins does not explicitly teach using DMA. Shaffer does teach using DMA (column 2, lines 50-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins. One of ordinary skill in the art would have been motivated to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins because Shaffer teaches the testing of memory modules in a system and reporting the errors therein (column 3, lines 19-31); an explicit desire of Jenkins (column 7, line 46 – column 8, line 39).

As per claim 17, Jenkins in view of Shaffer the computer system of claim 15 further comprising: an operating system; wherein the processor is configured to cause the operating system to be executed, and wherein the test module is configured to cause the tests to be performed on the memory during execution of the operating system (column 3, lines 24-39;

column 4, 32-34). Jenkins does not explicitly teach using DMA. Shaffer does teach using DMA (column 2, lines 50-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins. One of ordinary skill in the art would have been motivated to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins because Shaffer teaches the testing of memory modules in a system and reporting the errors therein (column 3, lines 19-31); an explicit desire of Jenkins (column 7, line 46 – column 8, line 39).

As per claim 18, Jenkins teaches the computer system of claim 15 wherein the bus comprises a system bus (column 3, lines 53-67).

As per claim 19, Jenkins in view of Shaffer teaches the computer system of claim 15. Shaffer teaches wherein the test transactions include read and write transactions (column 1, lines 44-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the R/W process of Shaffer in the general testing process of Jenkins. One of ordinary skill in the art would have been motivated to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins because Shaffer teaches the testing of memory modules in a system and reporting the errors therein (column 3, lines 19-31); an explicit desire of Jenkins (column 7, line 46 – column 8, line 39).

As per claim 20, Jenkins in view of Shaffer teaches the computer system of claim 19, Shaffer teaches wherein the read and write transactions comprise direct memory access (DMA) transactions (column 2, lines 50-56). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins. One of ordinary skill in the art would have been motivated to

use the R/W and DMA testing process of Shaffer in the general testing process of Jenkins because Shaffer teaches the testing of memory modules in a system and reporting the errors therein (column 3, lines 19-31); an explicit desire of Jenkins (column 7, line 46 – column 8, line 39).

Allowable Subject Matter

5. Claims 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 6/20/07 have been fully considered but they are not persuasive.

With respect to claim 1, the applicant has amended the claim to provide to the first I/O controller to cause the tests to be performed on the memory. The applicant has argued that Jenkins teaches away from this newly added limitation. The examiner respectfully disagrees. Jenkins teaches in column 7, table 3 many different memories that are tested. One such memory that is tested is the floppy drive. Looking at figure 1, it is clear to see that the floppy drive (140) is connected to the I/O controller. Since the test module (150) is connected through the I/O controller to the floppy memory drive, it is interpreted that the test module does provide the I/O

controller with test transactions to be performed on the floppy using a first bus. If the applicant wishes to better explain any direct connections and detailed first buses, he is urged to do so.

With respect to the USC 103 rejections, the applicant has argued that Shaffer is not combinable with Jenkins in that it involves changing the principle operation of Jenkins. The examiner respectfully disagrees. The examiner contends that this combination of the DMA transactions of Shaffer would further enhance the functionality of Jenkins. For instance, Jenkins mentions in column 3, lines 55-57, the use of a DMA controller with respect to the connection of the test module. The examiner brought in Shaffer to fulfill the functions that the DMA could have utilized, but was not further detailed in the invention of Jenkins.

In light of the above arguments, all applicable rejected claims stand.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christopher S. McCarthy
Examiner
Art Unit 2113